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	Subsystem/Office Anti-Coincidence Detector Subsystem	
Document Title **GLAST LAT ACD GAFE ASIC Test Plan & Procedures**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Anti-Coincidence Detector (ACD)

GLAST ACD Front-end Electronics (GAFE) ASIC

Test Plan & Procedures

DRAFT

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
1.0	07/07/2002	Re-format the Satpal's original document
2.0	11/04/2002	Contents enriched and sectioning changed
3.0	***January 10, 2003***	***Re-Engineered Document***

Table of Contents

1 Purpose

This document describes the ***plans and*** procedures of the electric tests on the GLAST ACD Front-end Electronics (GAFE) ASIC's before and after their assembly onto an ACD FREE card.

2 Definitions and Acronyms

ACD	The LAT Anti-Coincidence Detector Subsystem
ADC	Analog-to-Digital Converter
AEM	ACD Electronics Module
ASIC	Application Specific Integrated Circuits
BEA	Base Electronics Assembly
CAL	The LAT Calorimeter Subsystem
DAQ	Data Acquisition
EGSE	Electrical Ground Support Equipment
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FM	Flight Module
FMEA	Failure Mode Effect Analysis
FREE	Front End Electronics
GAFE	GLAST ACD Front End – Analog ASIC
GARC	GLAST ACD Readout Controller – Digital ASIC
GEVS	General Environmental Verification Specification
GLAST	Gamma-ray Large Area Space Telescope
HVBS	High Voltage Bias Supply
ICD	Interface Control Document
IDT	Instrument Development Team
I&T	Integration and Test
IRD	Interface Requirements Document
JSC	Johnson Space Center
LAT	Large Area Telescope
MGSE	Mechanical Ground Support Equipment
MLI	Multi-Layer Insulation
MPLS	Multi-purpose Lift Sling
PCB	Printed Circuit Board

PDR	Preliminary Design Review
PMT	Photomultiplier Tube
PVM	Performance Verification Matrix
QA	Quality Assurance
SCL	Spacecraft Command Language
SEL	Single Event Latch-up
SEU	Single Event Upset
SLAC	Stanford Linear Accelorator Center
TACK	Trigger Acknowledge
TDA	Tile Detector Assembly
T&DF	Trigger and Data Flow Subsystem (LAT)
TBD	To Be Determined
TBR	To Be Resolved
TSA	Tile Shell Assembly
TSS	Thermal Synthesizer System
TKR	The LAT Tracker Subsystem
VME	Versa Module Eurocard
WBS	Work Breakdown Structure
WOA	Work Order Authorization

3 Applicable Documents

Documents relevant to the ACD GAFE ASIC test plan include the following.

1. LAT-SS-00016, LAT ACD Subsystem Requirements – Level III Specification
2. LAT-SS-00352, LAT ACD Electronics Requirements – Level IV Specification
3. LAT-SS-00437, LAT ACD Mechanical Requirements – Level IV Specification
4. LAT-MD-00039-01, LAT Performance Assurance Implementation Plan (PAIP)
5. LAT-MD-00099-002, LAT EEE Parts Program Control Plan
6. LAT-SS-00107-1, LAT Mechanical Parts Plan
7. LAT-MD-00078-01, LAT System Safety Program Plan (SSPP)
8. ACD-QA-8001, ACD Quality Plan
9. GSFC-663-ACD-000, LAT ACD Electronics Specifications

4 Introduction

The Gamma-Ray Large Area Space Telescope (GLAST) Anti-Coincidence Detector (ACD) Front-End (GAFE) Application Specific Integrated Circuit (ASIC) ***is the*** analog front-end electronics that receives signals from a PMT viewing an ACD tile (or a scintillation fiber ribbon) and processes them to generate various discriminator outputs. It also shapes, holds, and digitizes the PMT signals for Pulse Height Analysis (PHA). It ***consists of*** the analog circuitry for signal processing; the DAC's to generate the various ***threshold and bias voltages***; and the digital circuitry to communicate with a GARC ASIC and digital interface of the LAT instrument electronics. The design of GAFE ASIC is described in detail in the LAT ACD Electronics Specifications, GSFC-663-ACD-000. The signal names and pins are defined as follows.

Name	Pin	Type	Dir	Description
VCC	1, 10	Power	In	Analog power, 3.3 V
AGND	2, 4, 6, 30, 32, 34	Power	In	Analog ground
DVDD	22, 35	Power	In	Digital power, 3.3 V
DGND	12, 43	Power	In	Digital ground
SALO	3	Signal	In	Slow Amp, Low energy input
SAHI	5	Signal	In	Slow Amp, High energy input
DISCIN	7	Signal	In	Discriminator channel input
VREF	8	Bias	In	2.5 V reference
MUXH	31	Signal	Out	Sample & hold output (multiplexed)
MUXSA	33	Signal	Out	Shaping amp output (multiplexed)
TCI	44	Signal	Out	Test charge injection output
AD0 AD1 AD2 AD3 AD4	27 28 29 40 41	CMOS	In	Chip address
REF A	9	CMOS	Out	Test Point
VETO	26	LVDS	Out	VETO output
CHNID	25	LVDS	Out	PHA channel selection
IRTN	24	LVDS	Out	Current return for LLD, VETO, and chnid
HLD1 HLD2	17 16	LVDS.	Out	High-level discriminator output
RESET	23	CMOS	In	Reset for digital circuitry
HOLD+ HOLD-	21 20	LVDS.	In	Hold input for sample & hold circuit; logic high = hold mode, logic low = tracking mode
STROB+ STROB-	19 18	LVDS.	In	Strobe input for on-chip test pulser; turning to logic high causes the charge injection
CMDD+ CMDD-	38 39	LVDS	In	Command data to the digital control module
CMDCK+ CMDCK-	36 37	LVDS	In	Command clock to the digital control module
RTND	13	CMOS	Out	Return data from the digital block
STATE0 STATE1	15 14	CMOS	Out	Test outputs from the digital circuitry; diagnosis purpose only
NC42 NC11	42 11	N/A	N/A	Spare pins

5 Overview of the GAFE tests

The GAFE ASIC *received from the vendor shall have the* die wire-bonded and packaged in **a XXX pin XX.X mm x XX.X mm plastic quad flatpack (ASAT QFP208B?)**. All packaged GAFE ASIC's will be *inspected as per GSFC QMS Standards; and* tested to confirm its full functionality and performance before being assembled on to an ACD FREE card. The *inspection and* test results will be fully recorded for future reference.

The packaged GAFE chips will be checked out in three steps: visual inspection, *functional and* performance verification, and temperature cycling. Brief descriptions of the test steps *are* given below. A *subset* of *functional and* performance tests will be applied only on selected chips. Temperature cycling *for the GAFE ASIC* will be exercised after *the chip is mounted* onto the ACD FREE card, and only selected FREE cards will be temperature-cycled.

Visual Inspection

The GAFE packages will be visually inspected for any physical damage, *such as bent pins, cracked package, discoloration due to chemical or liquid abrasives etc*.

Functional & Performance test

The GAFE chips will be electrically tested its functionality and performance of both the analog and the digital sections. This document describes the test plan for *these sections and outlines the procedures to test the chips in accordance with the plan*. The test plan for the digital section *is based on the document developed by* Dave Sheppard (**document number, e.g. LAT-TD-00XXX**).

Temperature cycling

After the GAFE chips have been tested and deemed 'good', they will be mounted on FREE cards. To ensure completeness, the *fully populated* FREE card will be checked its functionality and performance in a range between -20 and +50 degree C.

***X* (# of chips)** GAFE's will be tested in *Y* working days; this makes a total time to test a single GAFE chip to be *Y/X* minutes, *which includes* handling of the chips and recording the results. Therefore, fully automated test system is needed for the performance test.

X chips	*Y* working days = *8Y* working hours
One chip	*X/480Y* minutes
Handling of a chip	5 minutes
Visual inspection	5 minutes
Functional & Performance Tests	10 minutes

Based on test results from the visual inspection and the *functional and* performance tests on packaged GAFE chips, the tested chips are either 1) to be assembled onto a FREE card, 2) to be rejected from the assembly (unused at all), or 3) to be stored as spares for future use.

6 *GAFE* Test Plan

The GAFE Test Plan consists of the Visual Inspection of the Test Setup and equipment therein, and will outline the Plan for testing the GAFE ASIC to verify the functionality and performance.

6.1 Visual inspection

The GAFE Test Board will be inspected for broken traces, cracks and unopened vias according to the criteria set down by GSFC Document TBD. These boards will be inspected again at the Fabrication Station prior to being populated. Once the boards have passed the visual inspection, they will be populated for 4 independent test channels, i.e. each channel will have a Zero Insertion Force (ZIF) receptacle for a GAFE Chip in the signal flow.

6.2 Functional & Performance test

The GAFE chips will be tested using ***this*** specially designed GAFE test board. During the ***functional &*** performance test, a GAFE chip will be mounted in a Zero Insertion Force (ZIF) socket on the test board. This type of mount increases the lead lengths, which is likely to make the critical analog front-end more susceptible to noise pick up, and increase the cross coupling between leads. However, it has the advantage of applying the least physical stress on the ASIC leads.

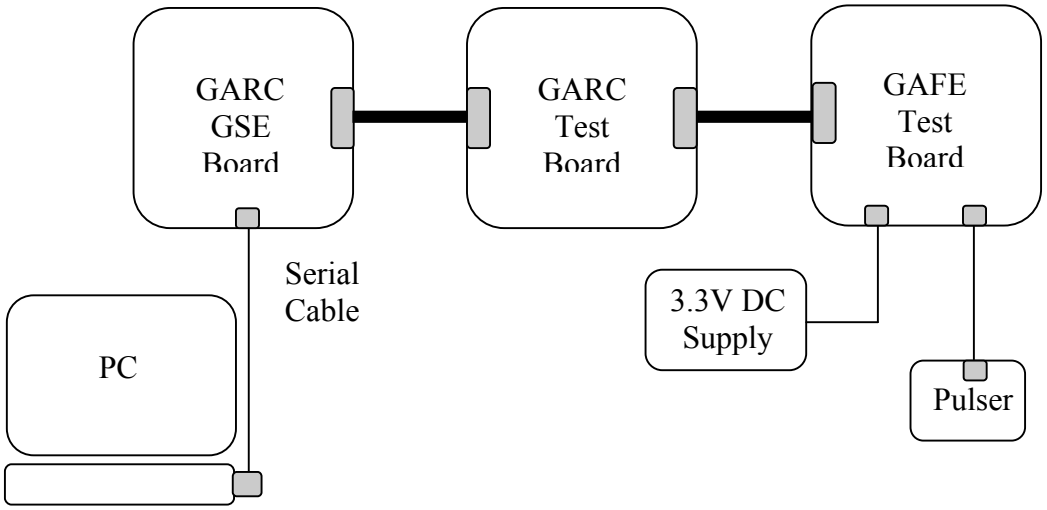


Fig. 1: Basic Test Set up using a GARC Test Board.

The GAFE test board will be controlled and read-out by a PC through specially designed interface boards. The PC will program and test the digital block on the GAFE, and read the ADC data from the GAFE test board. The ADC data ***will be*** plotted to check for linearity, and the standard deviation calculated to measure the ***associated*** noise. ***Currently,*** there are two configurations of GAFE test setup: one with a GARC Test ***& GSE*** Boards and the other with a ***GAFE Simulated GARC GSE Board***.

Test setup with GARC test board: The GAFE test board is connected to the GARC test board through a ***custom-made*** cable. The GARC test board is ***in turn*** connected to the GARC GSE board, which in turn hooks to the PC via a serial link.

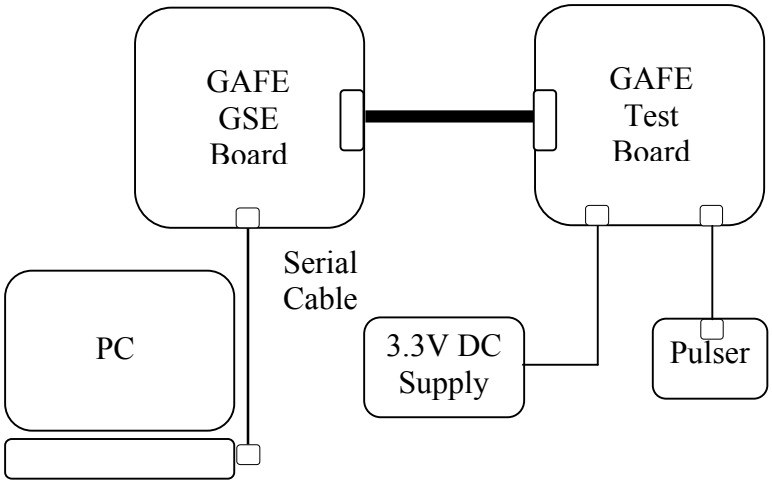


Fig. 2: Basic Test Set up using a GAFE Simulated GARC GSE Board.

Test setup with *GAFE Simulated GARC GSE Board*: This is alternative to the above; it uses a GAFE ***Simulated GARC*** GSE board rather than the GARC test board. The ***GAFE Simulated GARC*** GSE board connects directly to the PC via a serial link.

7 *GAFE* Test Procedures

The GAFE Test Procedures consist of Physical Procedures such as the visual inspection, and Electrical Test Procedures to verify and validate the functions and performance of the GAFE ASIC.

7.1 Visual Inspection

The GAFE chips will be inspected in accordance to guidelines described in TBD. Essentially, they will involve the visual inspection under a microscope for visible external damage. The extent of the damage shall include but not be limited to cracked package, broken pins, shorted pins, broken pins, missing pins, and mislabeled devices.
Once the GAFE chips have passed the visual inspection process, they will be isolated and stored for the testing process. The chips that fail the inspection process will be sorted into groups identified by the extent or description of their deficiencies and returned to the vendor for replacement.

7.2 Functional & Performance Test Procedures

The GAFE ASIC consists of the analog circuitry for signal processing; the DAC's to generate the various threshold and bias voltages; and the digital circuitry to communicate with a GARC ASIC and digital interface of the LAT instrument electronics.

The Analog Test Procedures will perform the functional and performance verification of the analog circuitry for signal processing and the DAC's. The Digital Test Procedures will perform the functional and performance verification of the interface between the GARC and the GAFE and the LAT instrument electronics and the GAFE.

All the Functional and Performance Test Procedures will be performed under the following conditions:

Supply voltage	VCC = 3.3 V, Vdd = 3.3 V
Bias	Vref = 2.5 V
Command clock	20 MHz
Temperature	XX – XX degree C

Prior to the test, the top half of the ZIF socket is opened, a GAFE chip dropped in place, and then the top half of the socket is clamped on to the chip to make the electrical connections.

7.2.1 Power measurements

This test will ensure that the current and power requirements of the GAFE ASIC were within the specified limits.

7.2.1.1 Setup

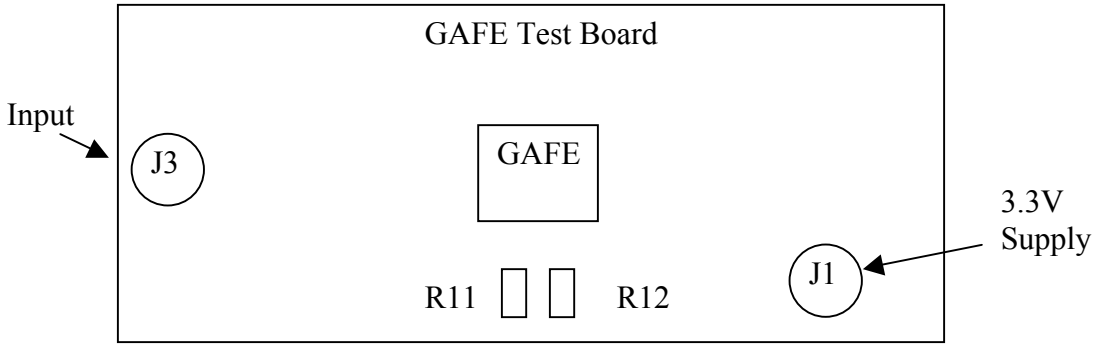
The test board is powered by 3.3v dc. VCC (analog supply), and Vdd (digital supply) are derived from the same 3.3v supply but isolated from each other by RC filtering of 100 ohms and 10uF tantalum paralleled with 0.1 ceramic capacitors.

7.2.1.2 Procedure

1. With the voltmeter, measure the voltage drops Vd and Va across the 100 ohm resistances R11 and R12 respectively.

The **Digital Power** is given as Vd * Vd / 100
The **Analog Power** is given as Va * Va / 100.

Where Vd = volt drop across R11 and Va = volt drop across R12.



7.3 Analogue Test Procedures

The following tests will verify and validate the analog functionality and performance. The tests are described in a procedural manner with the 'what is to be tested', 'what will be measured' and 'how the results will be verified'. Furthermore, the tests will provide the 'what has to be tested' for the Automated Test Procedures. The tests will verify that the GAFE meets the ACD Level IV Electronics Requirements, LAT-SS-00352, and the ACD-LAT Interface Control Document, LAT-SS-00-363. The Level IV Requirements are shown in Appendix A.

7.3.1 Shaping Amp Test Procedures

This test is to measure the Shaping Amp Gain to an incrementing Pulse Input and the corresponding Peaking Time.

7.3.1.1 Setup

The configuration of the test board for these tests requires C10, C11, R22, not to be populated; and R17 to be replaced by a 33pf capacitor. The above components are located adjacent to the coax connector J3. For this test the charge injection will be done through the 33pf mounted in place of R17. This is required as the charge injected through a smaller capacitance will be too small to cover the entire dynamic range of the ASIC; also, a larger capacitance helps keep down the effects due to parasitics.

1. Set a standard Tail Pulse generator to a rise time of 100 ns or less, fall time of 500 us or more, and set the output to inverted so as to get an inverted exponential pulse shape. Set the pulser rep rate to 100 pulses per sec.
2. Connect the shaped amp output at MUXSA at test point TP1 to a digital scope set to average 1000 pulses.
3. On to another input channel of the scope connect the input pulse from the tail pulser.

7.3.1.2 Shaping Amp – Low Signal Test Procedures

1. From the PC connected to the GSE board, issue the command to select the High gain channel.
2. Step the pulser output for Low Signal, i.e. from 25mv to 250mv; in steps of 25 mv, this would cover a range up to 12.9 MIPs.
3. Set the pulser output to 25 mv. Measure the mean amplitude on the digital scope of the shaped amp output for a 1000 pulses, also measure the input on the second channel of the scope.
4. Issue the command from the PC to switch to the low gain channel and measure the mean amplitude for the shaped output.
5. Increment the pulser output by 25 mv
6. Issue the PC command to select the High gain channel, and repeat the above measurements.
7. Repeat the above sequence of steps till the pulser is stepped from 25 mv to 250 mv in steps of 25 mv.
8. Plot the input versus output for the low gain and high gain channels.

7.3.1.3 Shaping Amp – High Signal Test Procedures

The pulser output is amplified by a gain of 2 by an external amplifier that can give 20 V Peak to peak swing.

1. Step the pulser output for High Signal, i.e. from 1v to 10v, in steps of 1v, the amplified output goes upto 20v or equivalently upto 1031.25 MIPs. The output of this amplifier is connected to the ASIC via jack J3 on the test board.
2. Issue the command from the PC to switch to the low gain channel and measure the mean amplitude for the shaped output.
3. Set the pulser output to 1v. Measure the mean amplitude on the digital scope of the shaped amp output for a 1000 pulses, also measure the input on the second channel of the scope.
4. Increment the pulser output by 1v
5. Repeat the above sequence of steps till the pulser is stepped from 1v to 10v in steps of 1v.
6. Plot the input versus output for the low gain channel.

7.3.2 Pulse Height Amplitude Linearity Test Procedures

These tests are performed to characterize the linearity of the Pulse Height Amplitude through the Shaping Amplifiers. They are performed using the option to inject a Test Charge via the Test DAC.

7.3.2.1 Setup

The configuration of the test board for these tests requires C10, C11, R22, not to be populated; and R17 to be replaced by a 33pf capacitor. The above components are located adjacent to the coax connector J3. For this test the charge injection will be done through the 33pf mounted in place of R17. This is required as the charge injected through a smaller capacitance will be too small to cover the entire dynamic range of the ASIC; also, a larger capacitance helps keep down the effects due to parasitics.

1. Connect the Shaping Amplifier Output at MUXSA at test point TP1 to a digital scope set to average 1000 pulses.

7.3.2.2 High Gain Channel Test Procedures

1. From the PC connected to the GSE board, issue the command to select the high gain channel.
2. Program the Test DAC to ***the*** minimum value.
3. From the GSE issue the "Test Strobe" command ***to be repeated*** at the rate of 100 times per second.
4. Measure the average value of the Shaped Pulse Output on the scope.
5. Increment the Test DAC by 5 till the DAC maximum is reached and at each setting repeat the above measurements.
6. ***Plot the DAC vs. Shaping Amplifier Output***.

7.3.2.3 Low Gain Channel Test Procedures

1. From the PC connected to the GSE board, issue the command to select the Low gain channel.
2. Program the Test DAC to ***the*** minimum value.
3. From the GSE issue the "Test Strobe" command ***to be repeated*** at the rate of 100 times per second.
4. Measure the average value of the shaped pulse on the scope.
5. Increment the Test DAC by 5 till the DAC maximum is reached and at each setting repeat the above measurements.
6. ***Plot the DAC vs. Shaping Amp Output***.

7.3.3 Sample and Hold Test Procedures

The Sample and Hold Test Procedures perform tests to check the Sample and Hold functionality and performance in response to a pulsed input to the input of the Shaping Amplifiers, and a delayed pulse to the Sample and Hold Outputs.

7.3.3.1 Setup

The configuration of the test board for these tests requires C10, C11, R22, not to be populated; and R17 to be replaced by a 33pf capacitor. The above components are located adjacent to the coax connector J3. For this test the charge injection will be done through the 33pf mounted in place of R17. This is required as the charge injected through a smaller capacitance will be too small to cover the entire dynamic range of the ASIC; also, a larger capacitance helps keep down the effects due to parasitics.

1. Set a standard Tail Pulse generator to a rise time of 100 ns or less, fall time of 500 us or more, and set the output to inverted so as to get an inverted exponential pulse shape. Set the pulser rep rate to 100 pulses per sec.
2. Connect the Peak Hold Output at either lead of resistance R5 to a digital scope set to average 1000 pulses.
3. On to another input channel of the scope connect the input pulse from the tail pulser.
4. The trigger output of the pulser set to be delayed by 4us is connected to the GSE board to enable the GSE board to generate a hold pulse to the GAFE ASIC.

7.3.3.2 Sample and Hold – Low Signal Test Procedures

1. From the PC connected to the GSE board, issue the command to select the high gain channel.
2. Step the pulser output from 25mv to 250mv; in steps of 25 mv, this would cover a range up to 12.9 MIPs.
3. Set the pulser output to 25 mv. Measure the mean amplitude on the digital scope of the track and hold output for a 1000 pulses, also measure the input on the second channel of the scope.
4. Issue the command from the PC to switch to the low gain channel and measure the mean amplitude for the hold output.
5. Increment the pulser output by 25 mv

6. Issue the PC command to select the High gain channel, and repeat the above measurements.
7. Repeat the above sequence of steps till the pulser is stepped from 25 mv to 250 mv in steps of 25 mv.
8. Plot the input versus output for the low gain and high gain channels.

7.3.3.3 Sample and Hold – High Signal Test Procedures

The pulser output is amplified by a gain of 2 by an external amplifier that can give 20 V Peak to peak swing.

1. Step the pulser output from 1v to 10v; in steps of 1v, the amplified output goes upto 20v or equivalently upto 1031.25 MIPs. The output of this amplifier is connected to the ASIC via jack J3 on the test board.
2. Issue the command from the PC to switch to the low gain channel and measure the mean amplitude for the hold output.
3. Set the pulser output to 1v. Measure the mean amplitude on the digital scope of the Track and hold output for 1000 pulses, also measure the input on the second channel of the scope.
4. Increment the pulser output by 1v
5. Repeat the above sequence of steps till the pulser is stepped from 1v to 10v in steps of 1v.
6. Plot the input versus output for the low gain channel.

7.3.4 Noise Measurements

The noise at the Shaping Amplifier Output is measured using a digital oscilloscope, and referred to the Input of the Shaping Amplifier based on the Gain. The corresponding MIP equivalent of the Noise is calculated and verified with the specifications.

7.3.4.1 Setup

The configuration of the test board for these tests requires C10, C11, R22, not to be populated; and R17 to be replaced by a 33pf capacitor. The above components are located adjacent to the coax connector J3.

1. Short the input lead of the 33pf mounted at location R17 to ground, this grounds the input for this test.
2. Connect the Shaping Amplifier Output at test point TP1 to a digital scope.

7.3.4.2 High Gain Channel Noise Test Procedures

1. From the PC connected to the GSE board, issue the command to select the High Gain channel.
2. The digital scope is used to measure the rms value, Vn, of the noise at the shaping amplifier output; the measurements made are in units of volts.

   If G = gain of High Gain channel in volts/Coulomb calculated in ***Test 7.3.2***, then the noise referred to the input is ***given by the following expression***:

Qn = Vn / G Coulombs = rms noise in coulombs referred to the input.

7.3.4.3 Low Gain Channel Noise Test Procedures

1. From the PC connected to the GSE board, issue the command to select the Low Gain channel.
2. The digital scope is used to measure the rms value, Vn, of the noise at the shaping amplifier output; the measurements made are in units of volts.

   If G = gain of Low Gain channel in volts/Coulomb calculated in ***Test 7.2.2***, then the noise referred to the input is ***given by the following expression:***

   Qn = Vn / G Coulombs = rms noise in coulombs referred to the input.

7.3.4.4 Input Noise Measurement Test Procedures

1. The probe of the digital scope is connected to input capacitor at the node connecting C10, R18 and R20. The rms noise, Vn, is measured on the digital scope.

   The noise in coulombs is ***given by the following expression:***

   Qn = Vn * Cap = Vn * 33Pf (since the input cap C10 = 33pf.)

7.3.5 VETO Discriminator and DAC Verification Tests

The VETO Discriminator and DAC Test Procedures perform tests to verify that the VETO Discriminator correctly compares the VETO DAC reference value with the input pulse height to correctly trigger the VETO Generator. Ideally the variation of the VETO DAC with the Pulse Height should be linear.

7.3.5.1 Setup

The configuration of the test board for these tests requires C10, C11, R22, not to be populated; and R17 to be replaced by a 33pf capacitor. The above components are located adjacent to the coax connector J3. For this test the charge injection will be done through the 33pf mounted in place of R17. This is required as the charge injected through a smaller capacitance will be too small to cover the entire dynamic range of the ASIC; also, a larger capacitance helps keep down the effects due to parasitics.

1. Set a standard Tail Pulse generator to a rise time of 100 ns or less, fall time of 500 us or more, and set the output to inverted so as to get an inverted exponential pulse shape. Set the pulse repetition rate to 100 pulses per sec.

7.3.5.2 VETO Discriminator Test Procedures

1. Connect the scope probes after the LVDS receiver on the GSE board.

2. Set the VETO DAC to 63 (closest to baseline) and raise the pulse amplitude of the Tail Pulse Generator, till the VETO just fires.
3. Change the VETO DAC by a count of 5 to 57 (higher threshold since the signal is inverted) and raise the pulse amplitude of the Tail Pulse Generator, till the VETO just fires.
4. Decrement the VETO DAC till it goes down to its minimum, and plot the graph of VETO DAC vs. Pulse Signal amplitude.

7.3.6 VETO Delay Measurements

This test measures the delay between the Input Tail Pulse and the VETO Output Pulse measured after the LVDS Receiver. The Discriminator Input Resistance Rdisc is varied between 11 Kilo Ohms and 120 Kilo Ohms to observe the variation in the delay. Ideally, the variation of the delay with the variation in the Discriminator Resistance Rdisc at the input of the VETO Discriminator should be a straight line.

7.3.6.1 Setup

The configuration of the test board for these tests requires C10, C11, R22, not to be populated; and R17 to be replaced by a 33pf capacitor. The above components are located adjacent to the coax connector J3. For this test the charge injection will be done through the 33pf mounted in place of R17. This is required as the charge injected through a smaller capacitance will be too small to cover the entire dynamic range of the ASIC; also, a larger capacitance helps keep down the effects due to parasitics.

1. Set a standard Tail Pulse generator to a rise time of 100 ns or less, fall time of 500 us or more, and set the output to inverted so as to get an inverted exponential pulse shape. Set the pulser repetition rate to 100 pulses per sec.

7.3.6.2 Delay Measurement Test Procedures

1. With Tail pulser signal turned off (i.e. set to zero), the VETO DAC threshold is varied (the DAC being settable both above and below the baseline to accommodate for the discriminator offset) till the VETO discriminator turns off.
2. Increment the DAC threshold Voltage by approximately 6.2 mV, corresponding to 0.3 MIP.
3. Set the Tail Pulser Signal Voltage to approximately 19.4 mV, corresponding to 1 MIP.
4. Measure the time delay between the Tail Pulse Input and the VETO Output measured after the LVDS receiver.

7.3.7 HLD Discriminator and DAC Verification Tests

The HLD Discriminator and DAC Test Procedures perform tests to verify that the HLD Discriminator correctly compares the HLD DAC reference value with the input pulse height to correctly trigger the HLD Generator. Ideally the variation of the HLD DAC with the Pulse Height should be linear.

7.3.7.1 Setup

The configuration of the test board for these tests requires C10, C11, R22, not to be populated; and R17 to be replaced by a 33pf capacitor. The above components are located adjacent to the coax connector J3. For this test the charge injection will be done through the 33pf mounted in place of R17. This is required as the charge injected through a smaller capacitance will be too small to cover the entire dynamic range of the ASIC; also, a larger capacitance helps keep down the effects due to parasitics.

1. Set a standard Tail Pulse generator to a rise time of 100 ns or less, fall time of 500 us or more, and set the output to inverted so as to get an inverted exponential pulse shape. Set the pulse repetition rate to 100 pulses per sec.

7.3.7.2 HLD Discriminator Test Procedures

1. Connect the scope probes after the LVDS receiver on the GSE board.
2. Set the HLD DAC to 63 (closest to the baseline) and raise the pulse amplitude of the Tail Pulse Generator, till the HLD just fires.
3. Change the HLD DAC by a count of 5 to 57 (higher threshold since the signal is inverted) and raise the pulse amplitude of the Tail Pulse Generator, till the HLD just fires.
4. Decrement the HLD DAC till it goes down to its minimum, and plot the graph of HLD DAC vs. signal amplitude.

7.3.8 Voltage Bias for Shaping Amplifiers Baseline Tests

This set of tests is to measure the baseline value of the Shaping Amplifier Outputs in response to the DAC settings of the Voltage Bias to the Shaping Amplifiers.

7.3.8.1 VBSA Test Procedures

1. Connect the scope probe to test point TP1, the Shaping Amplifier Output.
2. Set the VBSA DAC to zero and measure the baseline at TP1 on the scope.
3. Increment the DAC and repeat measurements till the DAC reaches its full value of 8.
4. Plot the VBSA DAC Output setting vs. Baseline Output measured at TP1.

7.3.9 Auto Channel Mode Select Tests

This set of tests verify that the chip automatically switches over from the High Gain channel for Low Input Signals to the Low Gain Channel for High Input Signals at the design threshold for the Low Gain Channel. These tests, further validates the switch-over through measurement of the Input Pulse Amplitude at the cross-over point.

7.3.9.1 Setup

The configuration of the test board for these tests requires C10, C11, R22, not to be populated; and R17 to be replaced by a 33pf capacitor. The above components are located adjacent to the coax connector J3. For this test the charge injection will be done through the 33pf mounted in place of R17. This is required as the charge injected through a smaller capacitance will be too small to cover the entire dynamic range of the ASIC; also, a larger capacitance helps keep down the effects due to parasitics.

1. Set a standard Tail Pulse generator to a rise time of 100 ns or less, fall time of 500 us or more, and set the output to inverted so as to get an inverted exponential pulse shape. Set the pulser rep rate to 100 pulses per sec.
2. Connect the Shaping Amplifier Output at MUXSA at test point TP1 to a digital scope.
3. On to another input channel of the scope connect the input pulse from the Tail Pulser.

7.3.9.2 Auto Channel Mode Select Test Procedures

1. From the PC connected to the GSE board, issue the command to select the low gain channel.
2. From the GSE, issue the command to operate the ASIC in "Auto Channel Mode".
3. Starting from zero volt Tail pulse, increase the signal amplitude and watch the MUXSA output increase from minimum towards maximum.
4. The Tail Pulser amplitude is increased to the point where the MUXSA suddenly changes from near maximum to near minimum value, which is when the automatic switch over from High Gain Channel to Low Gain channel has occurred. The amplitude of the input pulse is measured at this point.

7.3.10 VETO Sensitivity Tests

This section has to be re-written to capture the criteria for allowable Sensitivity in terms of mV and pC. …

7.3.11 VETO – DAC Sensitivity

These tests will measure the GAFE sensitivity to step changes in the VETO DAC. The sensitivity should be within 0.05 MIP per step change in the VETO DAC.

7.3.11.1 Setup

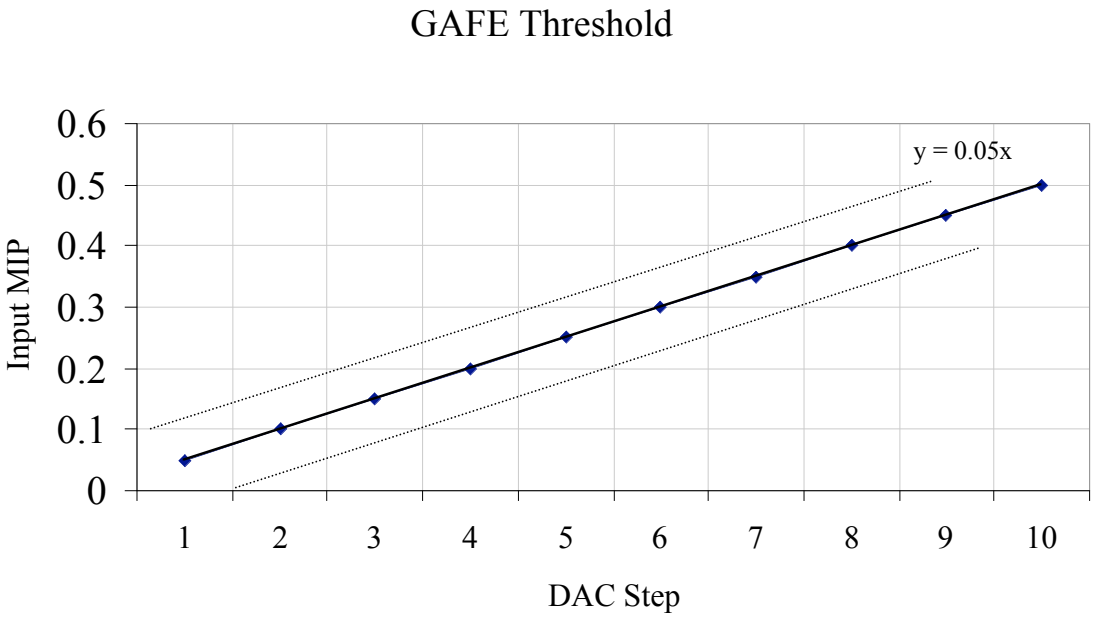
The configuration of the test board for these tests requires C10, C11, R22, not to be populated; and R17 to be replaced by a 33pf capacitor. The above components are located adjacent to the coax connector J3. For this test the charge injection will be done through the 33pf mounted in place of R17. This is required as the charge injected through a smaller capacitance will be too small to cover the entire dynamic range of the ASIC; also, a larger capacitance helps keep down the effects due to parasitics.

1. *Set a standard Tail Pulse generator to a rise time of 100 ns or less, fall time of 500 us or more, and set the output to inverted so as to get an inverted exponential pulse shape. Set the pulser repetition rate to 100 pulses per sec.*

7.3.11.2 VETO DAC Threshold Measurement Test Procedures

1. *With Tail pulser signal turned off (i.e. set to zero), the VETO DAC threshold is varied (the DAC being settable both above and below the baseline to accommodate for the discriminator offset) till the VETO discriminator turns off.*
2. *Increment the DAC threshold Voltage by approximately 6.2 mV, corresponding to 0.3 MIP.*

3. *Set the Tail Pulser Signal Voltage to approximately 19.4 mV, corresponding to 1 MIP.*
4. *Record the Tail Pulser Voltage when the VETO triggers for specific values of the VETO DAC.*
5. *Plot the Tail Pulser Voltage (Input) versus the VETO DAC setting.*
6. *Verify that the plot is within TBD of the ideal straight line corresponding to a slope of 0.05 MIP (0.97 mV) per VETO DAC threshold step (6.2 mV).*



7.4 Digital Test Procedures

The following tests will verify and validate the digital functionality and performance. The tests are described in a procedural manner with the 'what is to be tested', 'what will be measured' and 'how the results will be verified'. The GAFE digital logic interfaces to the ACD Readout Controller ASIC (GARC), which is the main logical interface for the ACD to the LAT instrument electronics. GARC provides the GAFE ASICs with commands and processes digital data returned from the logic core. Furthermore, the tests will provide the 'what has to be tested' for the Automated Test Procedures. The tests will verify that the GAFE meets the ACD Level IV Electronics Requirements, LAT-SS-00352, and the ACD-LAT Interface Control Document, LAT-SS-00-363. The Level IV Requirements are shown in Appendix A.

7.4.1 GAFE Digital Logic Tests:

The following list of commands is used by the GAFE logic to Read and Write to the GAFE Configuration Registers.

GAFE Cmd No.	ACD Command Mnemonic	Rd/Wr Status	Select GARC=0 GAFE=1	Function Block	Register Number	No. of Data Bits	Command Function
1	GAFE_Mode_Wr	W	1	GAFE Addr	0	16	Writes the GAFE mode register for the ASIC addressed
2	GAFE_Mode_Rd	R	1	GAFE Addr	0	16	Reads the GAFE mode register contents for the ASIC addressed
3	GAFE_DAC1_Wr	W	1	GAFE Addr	1	6	Writes the DAC1 register in the GAFE addressed
4	GAFE_DAC1_Rd	R	1	GAFE Addr	1	6	Reads back the contents of the DAC1 register in the addressed GAFE
5	GAFE_DAC2_Wr	W	1	GAFE Addr	2	6	Writes the DAC2 register in the GAFE addressed
6	GAFE_DAC2_Rd	R	1	GAFE Addr	2	6	Reads back the contents of the DAC2 register in the addressed GAFE
7	GAFE_DAC3_Wr	W	1	GAFE Addr	3	6	Writes the DAC3 register in the GAFE addressed
8	GAFE_DAC3_Rd	R	1	GAFE Addr	3	6	Reads back the contents of the DAC3 register in the addressed GAFE
9	GAFE_DAC4_Wr	W	1	GAFE Addr	4	6	Writes the DAC4 register in the GAFE addressed
10	GAFE_DAC4_Rd	R	1	GAFE Addr	4	6	Reads back the contents of the DAC4 register in the addressed GAFE
11	GAFE_DAC5_Wr	W	1	GAFE Addr	5	6	Writes the DAC5 register in the GAFE addressed
12	GAFE_DAC5_Rd	R	1	GAFE Addr	5	6	Reads back the contents of the DAC5 register in the addressed GAFE
13	GAFE_Version	R	1	GAFE Addr	6	3	Reads back the GAFE ASIC version
14	GAFE_Write_Ctr	R	1	GAFE Addr	7	8	Reads back the contents of the GAFE write counter register
15	GAFE_Reject_Ctr	R	1	GAFE Addr	8	8	Reads back the contents of the GAFE command reject register
16	GAFE_Cmd_Ctr	R	1	GAFE Addr	9	8	Reads back the contents of the GAFE command counter
17	GAFE_Chip_Addr	R	1	GAFE Addr	10	5	Reads back the hardwired address of a GAFE ASIC

7.4.1.1 Setup

The GAFE logic is based on a command-response protocol and requires a GARC or GARC simulator to access the logic functions. For each of the following commands, the proper GAFE logic response was tested. The test setup used is detailed in the diagram below. A GARC Version 1 ASIC mounted in the GARC test board was used as the GAFE interface.

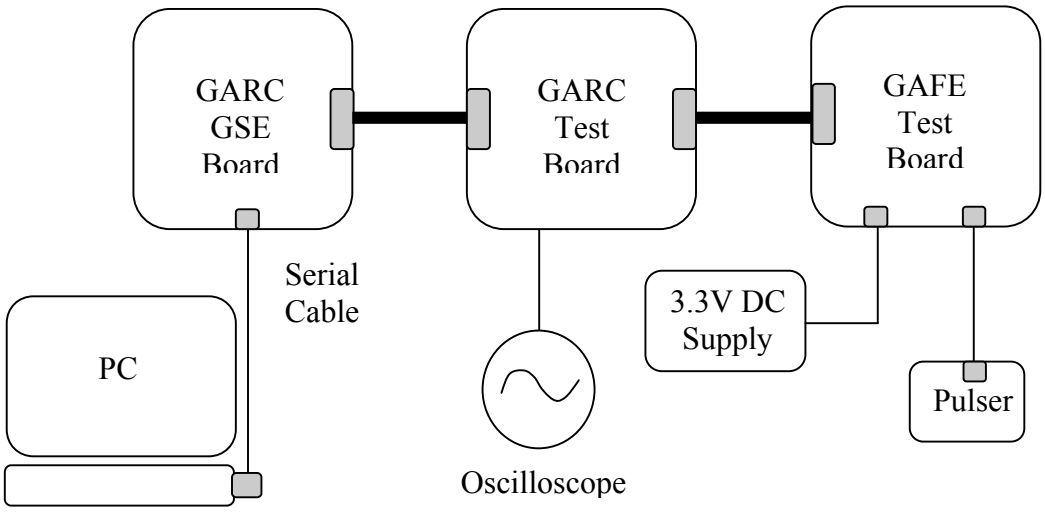


Figure 3. GAFE Digital Logic Tests with GSE Emulator

7.4.1.2 GAFE Digital Logic - Initial Reset Test Procedures

This section will verify that GAFE registers were properly initialized during a reset. Using a software program, (Bob Baker's AEM3.exe program), as the command and read-back software, the following register contents are read-back directly after reset. The values after a Reset are listed in the following table.

GAFE #2 Register	Read-back (dec)	Read-back (hex)
0	48	30
1	57	39
2	38	26
3	55	37
4	32	20
5	0	0
6	2	2
7	0	0
8	0	0
9	9	9
10	0	0

7.4.1.3 GAFE Digital Logic - Register Read/Write Test Procedures

All the registers in the GAFE Digital Module are tested for proper read and write response. The following registers, write and read back commands have to be verified.

Write Commands	Value	Read Commands	Value	Pass Criteria
GAFE_Mode_Write	0x00	GAFE_Mode_Read	0x00	Match
GAFE_Mode_Write	0x255	GAFE_Mode_Read	0x255	Match
GAFE_Mode_Write	0x48	GAFE_Mode_Read	0x48	Match
GAFE_DAC1_Write	0x00	GAFE_DAC1_Read	0x00	Match
GAFE_DAC1_Write	0x63	GAFE_DAC1_Read	0x63	Match
GAFE_DAC1_Write	0x57	GAFE_DAC1_Read	0x57	Match
GAFE_DAC2_Write	0x00	GAFE_DAC2_Read	0x00	Match
GAFE_DAC2_Write	0x63	GAFE_DAC2_Read	0x63	Match
GAFE_DAC2_Write	0x57	GAFE_DAC2_Read	0x57	Match
GAFE_DAC3_Write	0x00	GAFE_DAC3_Read	0x00	Match
GAFE_DAC3_Write	0x63	GAFE_DAC3_Read	0x63	Match
GAFE_DAC3_Write	0x55	GAFE_DAC3_Read	0x55	Match
GAFE_DAC4_Write	0x00	GAFE_DAC4_Read	0x00	Match
GAFE_DAC4_Write	0x63	GAFE_DAC4_Read	0x63	Match
GAFE_DAC4_Write	0x32	GAFE_DAC4_Read	0x32	Match
GAFE_DAC5_Write	0x00	GAFE_DAC5_Read	0x00	Match
GAFE_DAC5_Write	0x63	GAFE_DAC5_Read	0x63	Match
GAFE_DAC5_Write	0x00	GAFE_DAC5_Read	0x00	Match

7.4.1.4 GAFE Digital Logic Read-Only Registers Test Procedures:

To verify that the Read-Only Registers are functioning correctly, the following Read-Only commands are executed and the results verified.

1. ***Record the number of Read and Writes from the previous test.***
2. ***Write a value of 0x63 to GAFE Register 5, with a GAFE_DAC5_Wr command.***
3. ***Repeat this command 64 times, times to verify the roll-over from 63 to 0.***
4. ***Read the GAFE Register 5, with a GAFE_DAC5_Rd command.***
5. ***Repeat this command 64 times, times to verify the roll-over from 63 to 0.***

The hard-wired chip addresses on a test board are 0, 1, 2 and 3.

6. ***In response to the GAFE_Chip_Addr command, read back the GAFE Register 10.***
7. ***Repeat Read Commands to the Broadcast address 0x1F 10 times. These should be counted in the GAFE_Reject_Ctr Register (GAFE Register 8), as rejected Commands***
8. ***Read the GAFE Register 6, this should return the corrct version number for the GAFE ASIC.***

Read Commands	Read –Only Registers	Pass Criteria
GAFE_Version	GAFE Addr: 6	Correct GAFE ASIC version
GAFE_Write_Ctr	GAFE Addr: 7	Correct count of the GAFE Write Commands
GAFE_Cmd_Ctr	GAFE Addr: 9	Correct counts of the GAFE Read Commands
GAFE_Reject_Ctr	GAFE Addr: 8	Correct counts of rejected GAFE commands
GAFE_Chip_Addr	GAFE Addr: 10	Correct hard-wired address of the GAFE ASIC

7.4.1.5 GAFE Digital Logic Clock-to-Data Delay Test Procedures

This test verifies that the delay between the positive edges of the GAFE Clock and GAFE Data received is within the design specification.

1. *On the GARC simulator board, measure the delay from the positive edge of the GAFE clock out to the positive edge of the GAFE data received. This delay should be approximately 30 nanoseconds for a nominal clock speed of 5 MHz.*

7.5 Automated Test Procedures:

This section will essentially list an optimized set of tests that will enable a automated process by which the GAFE ASIC is tested in a short period of time to validate it's "GOODNESS". To do so it is essential that the important functionality and performance of the GAFE are verified and preserved.

7.5.1 Overview

The Digital Test Procedures for all the ASICs will be performed using the test set-up shown in Figure TBS. The GAFE ASIC will be powered up and the software script Automated Digital SW module (modified version of Bob's Software) executed. The results from the tests will be recorded in a file. However, any ASIC not meeting the criteria will be flagged in Real Time on the PC Screen. This will enable the sorting of the ASICs into 'GOOD' and 'OTHER' devices.

7.5.2 Functional & Performance Test Procedures for GOOD ASICs

For the sorted 'GOOD' chips, the linearity will be measured at the output of shaping amp, at the output of sample and hold, and finally from the ADC output with the ADC connected to the GAFE sample and hold output. For screening of GAFE chips in large number with an automated system, only the ADC output will be used to check the linearity and noise.

Glenn/Bob…..More to come.

7.6 Temperature Cycling

The Test Board will be put in a thermal Chamber and cycled over -20 deg C to + 50 deg C and the gain, linearity and noise of the high and low gain channels will be checked at different temperatures.

1. Set the test board in the thermal chamber and set the temperature to +25C.
2. After a steady temperature is reached, let the circuit soak for another hour and perform tests *described in Section 7.3 through Section 7.4.*
3. Repeat the tests for +50C
4. Repeat the tests for -20C
5. Repeat the tests for 0c.
6. Heat the chamber to above room temperature before opening the chamber door.

8 Chip rating and acceptance criteria

All tested GAFE chips are rated in three ranks based on the results from the visual inspection and the performance tests. Depending on its chip rating, a tested chip is to be assembled onto a FREE card, rejected from the assembly (unused at all), or stored as spares for possible future use. The three ranks are described below.

1) **"Good":** Chips that pass the visual inspection and all the *functional and* performance tests. Chips rated "good" are primarily used to assemble a FREE card.

2) **"Spare":** Chips that pass the visual inspection and all the *functional and* performance tests except for the followings: **TBD** (e.g., channel gain is **TBS %** larger or smaller than the nominal value.)
3) **"Rejected":** Chips that are not rated either "good" or "spare". Chips rated "rejected" are not assembled onto a FREE card.

9 Appendix A

GAFE Requirements

System Level	*An AC-coupled input from the PMT*
Level IV Requirement 5.3	*Adjustable Threshold on VETO Detection of Charged Particles. The threshold for detecting charged particles shall be adjustable from 0.064 to 1.28 pC (0.1 to 2 MIP), with a step size of <0.032 pC (0.05 MIP).*
Level IV Requirement 5.4	*False VETO due to Electrical Noise. The total ACD false VETO trigger rate due to noise shall be less than 10 kHz (~46Hz per channel) at 0.096 pC (0.15 MIP) threshold (assuming 1 us VETO pulses).*
Level IV Requirement 5.5	*High Threshold Detection. The ACD shall detect pulses due to highly-ionizing particles, carbon-nitrogen-oxygen or heavier nuclei, denoted High-Level Threshold or High-Level Discriminator (HLD), which produce signals from 20 pC to 128 pC (31.2 - 200 MIP with a goal of 1000 MIPs).*
Level IV Requirement 5.6	*Adjustable High-Threshold. The High-Level Threshold shall be adjustable for PMT signals from 12.8 to 40.96 pC (20 to 64 MIP) in steps of 0.64 ± 20% pC (1 ± 0.2 MIP).*
Level IV Requirement 5.8.3	*Fast VETO Re-triggering. The Fast VETO discriminator shall be capable of re-triggering less than 50 ns after the trailing edge of the VETO output signal.*
Level IV Requirement 5.9.8	*Test Pulse Injection. For test purposes, the ACD electronics shall incorporate the capability to be artificially stimulated by a test charge, via commands. The test charge injection range shall be 0 - 200 MIP with a goal of 0 - 1000 MIP.*
Level IV Requirement 5.9.5	*Integral non-linearity. The integral non-linearity should be kept reasonably low (defined as ~ < 2% over the top 95% of the signal input range), for ease of analysis.*
Level IV Requirement 5.9.6	*The differential non-linearity should be kept reasonably low (defined as approximately no more than +/- 1/2 LSB, or 1/2048 of full scale, whichever is greater, over the middle 95% of the signal input range) for ease of analysis.*
Level IV Requirement 5.9.7	*The analog signal processing chain shall exhibit temperature stability of gain better than 500 ppm per degree C over the operating temperature range. For both the low range (0 to 6.4 pC, = 10 MIPs) and the high range (6.4 to 640 pC, 10 to 200 MIPs, the requirement is 200 MIPs but designed to 1000 MIPs),*

	the analog signal processing chain shall exhibit temperature stability of its baseline better than 0.05% of full scale per degree C.